METHOD AND APPARATUS FOR ADAPTING WRITE INSTRUCTIONS FOR AN EXPANSION BUS

ABSTRACT

A method and apparatus for adapting write instructions for an expansion bus are described herein. In one embodiment, the method includes commencing execution of a first set of one or more write instructions, wherein the write instructions of the first set are the width of a processor data bus. The method also includes aborting the execution of the first set of write instructions. In response to the aborting, the method includes creating a second set of one or more write instructions, wherein the write instructions of the second set are the width of an expansion bus and executing the second set of write instructions.

In one embodiment, the apparatus includes a memory management unit to receive a virtual address and determine whether the virtual address maps to an inaccessible physical address. The memory management unit is to transmit an abort indication if the virtual address maps to an inaccessible address. The apparatus also includes a processor core to receive the abort indication from the memory management unit and to execute instructions. In the apparatus, the processor core includes an abort handler to create new instructions in response to receipt of the abort indication, wherein the new instructions are the width of an expansion bus.